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Single-event Upsets (SEUs) Induced by Heavy Ions in 14-nm FinFET SRAM

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Abstract: The characteristic of single-event upset(SEU) in a 14-nm bulk fin field-effect transistor (Fin-FET) static random access memory(SRAM) is investigated by heavy-ion experiments. The linear energy transfer(LET) threshold $0.1 \,\text{MeV}/(\text{mg/cm}^2)$ is obtained by fitting the SEU cross-section using the Weibull function. The contribution of multiple-bit upset(MBU) is investigated. The results show that when the LET is equal to $40.3 \,\text{MeV}/(\text{mg/cm}^2)$, greater than 95% of SEU comes from the MBU. Additionally, the SEU cross-section of the FinFET SRAM presents anisotropies for incident angles associated with the fin direction. This research has a certain kind of guiding role in designing of radiation-hardened complementary metal-oxide semiconductor(CMOS) integrated circuits(ICs) based on FinFET technology.

Key words: FinFET SRAM; heavy ion; single-event upset(SEU); angle effect

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1 Introduction

With the development of technology, more and more electronic devices are highly in demand for space and other radiation environments. However, the radiation effect to devices caused by energetic particles has become the main reason for the failure/damage of the on-orbit spacecrafts equipped with advance technology and modern electronic devices^[1]. The singleevent effect(SEE) is one of the major concerns in reliability issues because it can be induced by the incidence of a single energetic $\text{particle}^{[2]}$. During the last decades, the development of the microelectronics industry has always followed Moore's law, and the feature size of the electronics devices has been reached a scaling limit point^[3]. The three dimension(3D) fin field-effect transistor(FinFET) structure has replaced planar structure and become the feature size of the semiconductor devices below $22 \,\mathrm{nm}^{[4]}$.

The structures of planar FET and FinFET are

shown in Fig. 1. The FinFET static random access memory(SRAM) has great application prospects in the aerospace fields due to its excellent electrostatic control^[5]. Previous researches have demonstrated that the FinFET technology has significant advantages over planar technology in single-event response resistance, especially for low linear energy transfer(LET) particles^[6-7].



Fig. 1 (color online)Sketches of the planar FET and $\operatorname{FinFET}^{[8]}$.

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However, advanced technologies bring new responses to the SEE. On the one hand, due to the elevated source-drain structure and low fin-to-fin distance, the inter-junction proximity is close for the FinFET device. This facilitates charge collection by multiple junctions in a single radiation strike, which may lead to a higher probability of multiple-bit upset(MBU). In memory circuits such as SRAM, the analysis of the impact of MBU is quite $\operatorname{crucial}^{[9-10]}$ for various mitigation technique choices such as the degree of column interleaving and selection of error correction codes(ECC). As SRAM density increases and dimension reduces, MBU becomes a critical issue for SRAM applications in space electronic devices. On the other hand, due to the shape of the transistor, previous studies have shown that the single-event response of bulk FinFET devices is related to the incident angle of the particles [11-12]. In this paper, the single-event upset(SEU) of the 14-nm FinFET SRAM irradiated by heavy ions with different LETs is presented. The MBU contribution is also analyzed. Additionally, the influence of the anisotropic structure of FinFET is considered when the incident angle is inclined.

2 Experimental details

2.1 Devices under test (DUTs)

The test devices were fabricated using a commercial 14-nm bulk FinFET complementary metal-oxidesemiconductor(CMOS) technology. The capacity of the SRAM array was 128 Mbits. The device's normal core logic supply voltage was 0.8V, and the IO voltage was 1.8V. The clock frequency was adjustable with a 5 MHz minimum value to meet system timing requirements. The area of one memory cell was approximately $0.067 \,\mu m^2$. The information about the device is listed in Table 1.

	Table 1	Information of the device.	
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Paraments	Value	
Technology	14 nm, FinFET CMOS, Flip-Chip Packaged	
Die area	$6.17~\mathrm{mm}\times17.87~\mathrm{mm}$	
Core voltage/IO voltage	0.8 V/1.8 V	
Array dimension	128 Mbits	
Cell area	0.18 $\mu\mathrm{m}$ \times 0.37 $\mu\mathrm{m}$	
Fin height/Fin width	45 nm/15 nm	
Fin pitch/Contacted gate pitch	$46~\mathrm{nm}/85~\mathrm{nm}$	

A homemade test system was consisted of a robust mainboard and a replaceable DUT board. The

main board receives the request command from the host. Data operations such as write/read/compare/ correct were performed to run the DUT. The motherboard use to read the current value of DUT in real time along-with a record of the detected error details. Then, it was being uploaded to the host through Ethernet as the communication port. The mainboard and DUT board can transmit signals and powers by 180 differential pairs- channels through four Samtec's high-speed connectors. There was no other device placed nearby the irradiation region. The current of the DUT power components was continuously monitored and displayed in real-time. Slight voltage variations were probed and multiplied by a precision resistor and current sense amplifier, which were afterward converted to a digital form that can be handled by an FPGA rely on a 12-bit ADC. The DUT currents were monitored at one-second intervals.

2.2 Experiments setup

The tests of heavy-ion irradiation were performed at the Heavy Ion Research Facility in Lanzhou (HIRFL) and HI-13 Tandem Accelerator in Beijing. Experiments were carried out with different broad beam ion species including 12 C, 19 F, 78 Kr and 86 Kr. The heavy ions' LET at the sensitive volume(SV) surface is range from 2.4 to $40.3 \text{ MeV}/(\text{mg/cm}^2)$. The detailed experimental parameters used in this experiment are provided in Table 2. The heavy ions' LET values and the projected ranges in silicon were calculated by the Stopping and Range of Ions in Matter (SRIM) software^[13]. All tests were conducted at a normal voltage of 0.8 V and room temperature.

Table 2 Parameters of Heavy Ions Used in the Exper-

11	nent.			
Terminal	Ion species	Energy*/ MeV	$\frac{\rm LET \ */}{\rm [MeV/(mg\cdot cm^{-2})]}$	$\frac{\rm Penetration~depth}{\rm range~in~Si/\mu m}$
HI-13	^{12}C	52	2.6	67
	19 F	47	6.3	28
HIRFL	⁷⁸ Kr	3578	12.7	775
		2210	17.4	373
	⁸⁶ Kr	1371	24.7	185
		904	30.6	112
		294	40.3	38

*At the surface of SV.

Additionally, the 78 Kr ions with initial energy 3751 MeV were carried out at different angles incidence relative to two axes: 30° , 45° and 60° , as shown in Fig. 2(d) and (e). Fig. 2 shows the fin structure and the incident angle relative to the fin structure. The BC axis is parallel to fin direction, and the angle of



the DUT around the BC axis is marked as α angle. The AB axis is perpendicular to fin direction, and the angle of the DUT around the AB axis is marked as β angle.

3 Results and analysis

3.1 The SEU cross-section and MBU contribution

The SEU cross-section (σ) in the unit of cm²/bit for a bulk FinFET SRAM can be calculated by the following equation:

$$\sigma = \frac{N}{N_{\rm b}} \times F \times {\rm cos}\theta,$$

where N represents the total number of errors, $N_{\rm b}$ is the number of bits in the device, θ is the angle of incidence, and F is the ion fluence in ions/cm². The SEU cross-section as a function of LET for 14-nm flipchip packaged bulk FinFET SRAM is shown in Fig. 3. Error bars in all the plots of this paper represent standard errors. The figure shows that the SEU crosssection increases with LET value even if the LET value is larger than 24.7 MeV/(mg/cm²). The LET threshold is 0.1 MeV/(mg/cm²) obtained by fitting the SEU cross-section using the Weibull function. The reason of section unsaturation is related to MBU. As shown in Fig. 4, the contribution of the MBU is obvi-



Fig. 3 (color online)The SEU cross-section of 14-nm FinFET SRAM versus the LET of incident heavy ions.



Fig. 4 (color online) The percentage of different upset patterns varies with the LET of incident heavy ions.

ous increasing with LET. In this figure, SBU presents single-bit upset. MBU-2 presents double-bit upsets. MBU-3 presents triple-bit upsets. MBU-4 presents quadruple-bit upsets. MBU-5 presents quintuple-bit upsets. With the increase of LET, the proportion of the SBU decreases, while the proportion of the maximum number of upsets increases. The proportion of the MBU between them always increases first and then decreases. As the LET equals to $2.4 \text{ MeV}/(\text{mg/cm}^2)$, most patterns of upset are the SBU. However, the contribution of the MBU is greater than 95%, which becomes the main SEU component when the LET is equal to $40.3 \text{ MeV}/(\text{mg/cm}^2)$.

In silicon-based SRAM devices, the dominant reasons for the MBU are charge sharing, bipolar amplification, secondary ions, and peripheral circuits^[14]. For bulk FinFET SRAM devices, charge sharing is the key point. Firstly, the diameter of charge deposition from a single heavy ion covers multiple sensitive units. Secondly, the deposited charge of the ions on the substrate, including the sub-fin, would influence the MBU through diffusion. And the charge collected from the substrate is limited due to the narrow connection between the drain and the substrate of the bulk FinFET device. The charge sharing is enhanced due to the influence region of the ion-track structure increasing with the LET. The radial distribution of charges generated around an ion-track is an important factor for MBU induced by high-LET ions, especially in nanoscale devices like the ones used in the current study. For the FinFET technology, the iontrack radius needs to be considered because it is larger than the device dimensions like gate length and fin width.

3.2 The dependence of SEU cross-section on incident angle

As shown in Fig. 2(d) and (e), with respect to the two different directions of the fin structure, three incident angles of ⁷⁸Kr ions with the same initial energy (3751 MeV) were used to investigate the impact of incident angles on SEU. The SEU cross-section versus incident angle is shown in Fig. 5. In this figure, the SEU cross-section increases with the angle of incidence. Perpendicular to the fin direction (α), from 0° to 60°, the SEU cross-section increased by only 1.5 times. While parallel to the fin direction (β), it is increased by 4.9 times. The phenomenon of increasing the SEU cross-section with the β angle is similar to that in a planar device. As shown in Fig. 6 and Fig. 7, when the incident angle is β , the charge deposition path in FinFET is similar to that in a planar device.

The uniqueness of the geometry structure of Fin-FET determines the characteristic of its angular effect. On the one hand, when the ions are incident at α angle as shown in Fig. 7(a), for most of the events,



Fig. 5 (color online) The SEU cross-section versus the incident angle of heavy ions.



Fig. 6 (color online)The cross-section view of traditional planar transistor.



edge effect (the track length of ion in the SV is not arc-cosine law) will occur because the SV of the Fin-FET device is narrow and high. This is different from the traditional planar device as shown in Fig. 6. It will drop the track length of the ions in the SV. The decrease of the ion track length in the SV may lead to the decrease of SEU cross-section due to the decrease/ drop of the collected charge. However, when the ions are incident at β angle, the track length of incident ions in the SV follows a similar trend of like planar bulk technologies as shown in Fig. 6 and Fig. 7(b). It will raise the track length of the ions in the SV for most of the events, which leads to an increase of the collected charge.

On the other hand, as the device is a flip chip package device, all the ions before reaching the SV must pass through the substrate- acting as a natural energy degrader. As shown in Fig. 8, the curve represents the LET of ⁷⁸Kr ion with an initial energy of 3751 MeV as a function of incident depth in silicon. With the increase of the incident angle, the traverse length of ions through the substrate increases, resulting in the increase of LET value for the ions reaching the SV surface. In summary, the inconsistent change of charge deposition path of ions in SV caused by the characteristics of SV shape is the reason for the SEU cross-section changed differently with α angle and β angle.





4 Summary

This work investigates the impacts of LET on the SEU cross-section and MBU contribution induced by heavy ions for 14-nm bulk FinFET SRAM. Based on the anisotropic structure of the FinFET, the impact of angular effects on SEU cross-section induced by heavy ions are also investigated. The results show that MBU is a critical issue for high-LET heavy ion irradiation, due to increasing SRAM device density and scaled dimensions. The SEU cross-section of 14-nm bulk Fin-FET SRAMs exhibits strong dependence on geometry and orientation. When the incident angle is parallel or is perpendicular to the direction of the fin direction, the variation trend of the SEU cross-section is inconsistent, which is different from the planar device. These results are useful to design of radiationhardened CMOS integrated circuits(ICs) in the Fin-FET technology, suggesting the requirement of future investigations to be carried out on the impacts of track dimension and charge sharing in FinFET SRAM.

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重离子在14-nm FinFET SRAM 器件引起的单粒子翻转

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摘要: 通过重离子实验研究了 14-nm FinFET 工艺静态随机存取存储器 (SRAM) 的单粒子翻转 (SEU) 特性。通过 使用 Weibull 函数拟合 SEU 截面获得该器件的线性能量转移 (LET) 阈值: 0.1 MeV/(mg/cm²)。对多位翻转 (MBU) 贡献的统计结果表明,当 LET 等于 40.3 MeV/(mg/cm²)时,MBU的占比超过 95%。此外,FinFET SRAM的 SEU 截面呈现出与Fin 相关的入射角度的各向异性。该研究对基于FinFET 工艺的抗辐射 CMOS 集成电路 (IC) 的 设计具有一定的指导作用。

关键词: FinFET SRAM; 重离子; 单粒子翻转; 角度效应

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